REMARKS

Claims 1, 7, 16, 17, 19-21, 23, 33-36, and 38 are pending. Claim 1 has been amended, and claim 36 has been cancelled with this response. Reconsideration of the application is respectfully requested for at least the following reasons.

I. INTERVIEW SUMMARY

David Potashnik and Leonardo Andujar had a phone interview on January 14, 2008. We discussed claims 1 and 16, and in particular the proper interpretation of the claim term "bond pad." Although we had a meaningful discussion, no agreement was reached.

II. REJECTION OF CLAIM 1 UNDER 35 U.S.C. § 103(a)

Claim 1 was rejected under §103(a) as obvious over U.S. Pat. No. 6,545,358 (Jeong) in view of U.S. Pat. No. 5,117,276 (Thomas) in view of U.S. Pat. No. 6,171,927 (Sung) and further in view of U.S. Pat. No. 5,827,782 (Shih). Claim 1 has been amended to include a "bond pad" limitation, which has previously been alleged to be taught by U.S. Pat. No. 6,218,282 (Buynoski) in the context of claim 16. Claim 1 is believed to be patentably distinguishable from the prior art for at least the following reasons.

i. Although Buynoski in Fig. 4 teaches a bond pad 41, this bond pad 41 does not include multiple vias are formed over the individual bond pad as recited in amended claim 1.

Previous office actions noted that Buynoski in Fig. 4 includes a bond pad 41. *See* Buynoski Fig. 4, col. 5, lines 65-67. However, because this bond pad 41 ***does not include multiple vias formed over it***, the bond pad 41 fails to establish the limitation highlighted above. Further, one of ordinary skill in the art would not combine this bond pad with relatively-thin metal interconnect lines of other references, because doing so would vastly increase the area of the resultant integrated circuit.

ii. The claim interpretation urged in the pending OA is inconsistent with the plain meaning of the term "bond pad" as understood by a person of ordinary skill in the art. Buynoski when reasonably interpreted does not teach a bond pad including multiple vias formed over it as recited in claim 1.

The pending Office Action (OA of 9/29/08) alleges that Buynoski teaches multiple vias formed over individual bond pads by stating: "Buynoski (e.g., fig. 4) shows an integrated circuit having multiple vias 1 formed over individual bond pads (metal 1)." OA of 9/29/08, page 5, item 11. As now set forth, the applicants respectfully disagree.

The claim interpretation urged in the pending OA (in which the metal 1 region is deemed a bond pad) ***is inconsistent with the plain meaning of the term 'bond pad' as understood by a person of ordinary skill in the art***. The MPEP sets forth the standard for interpreting patent claims during prosecution as follows: "[a]lthough claims of issued patents are to be interpreted in light of the specification, prosecution history, prior art and other claims, ... [d]uring examination the claims must be interpreted as broadly as their claims reasonably allow. ... This means that the words of the claim must be given their plain meaning unless the plain meaning is inconsistent with the specification. MPEP 2111.01 (quoting text under Heading I). "'Plain meaning' refers to the *ordinary and customary meaning given to the term by those of ordinary skill in the art.*" MPEP 2111.01 (quoting Heading III) (emphasis added).

Consistent with the plain meaning of the term "bond pad", one of ordinary skill in the art appreciates that a "bond pad" is a relatively large-area feature of an integrated circuit by which external wires or circuit elements are typically coupled to an external surface of the die. Sematech, which provides an online technical dictionary, defines "bond pad" as "*relatively large metal areas* on a die used for electrical contact with a package or probe pins" (accessed at http://www.sematech.org/publications/dictionary/b.htm on Jan. 16, 2008). *See also* Appendix I of this response (providing a consistent definition of "bond pad" as supplied by the Examiner). Although the precise areas and features of bond pads may vary depending on the particular implementation used,

these definitions provide some evidence of what a person of ordinary skill understands a bond pad to be.

The metal 1 region of Buynoski is not a "bond pad" for several reasons. For example, metal 1 in Buynoski consists of ***thin lines*** used for local interconnect between closely spaced device features (e.g., source/drain regions). Bond pads, by contrast, require an area that is ***sufficiently large*** for physically bonding an external electrical connection to the integrated circuit. Because integrated circuit manufacturers want to maximize the density of device features per unit area, ***one of ordinary skill in the art would not insert a bond pad in place of Buynoski's metal 1 layer, because doing so would vastly increase the silicon footprint for each unit cell.*** Therefore, the proposed interpretation would result in the area of each unit cell increasing dramatically, thereby significantly raising the overall cost and/or significantly reducing the functionality of the integrated circuit.

Thus, because the metal 1 lines in Buynoski are not compatible with structural features of a bond pad, the claim interpretation given to "bond pad" in pending OA is contrary to the plain meaning of "bond pad" as understood by a person of ordinary skill in the art. When "bond pad" is given its proper interpretation, it is clear that Buynoski does not teach a bond pad including multiple vias formed over it as recited in claim 1. The other references fail to recite a bond pad in any respect, let alone a bond pad having multiple vias formed over it. Therefore, because this limitation is not established by the prior art of record and because there is no suggestion or motivation to modify the prior art to include this limitation, the applicants request withdrawal of the §103 rejection.

iii. Even if the OA's interpretation of "bond pad" is consistent with the plain meaning of "bond pad" as understood one of ordinary skill in the art (it is not consistent as set forth above), such an interpretation is clearly inconsistent with the specification.

As mentioned above from the MPEP 2111.01: "the words of the claim must be given their plain meaning ***unless the plain meaning is inconsistent with the***

specification. *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989)." Therefore, even if the pending OA's interpretation is consistent with the plain meaning (which it is not as set forth above), ***the plain meaning would have to be abandoned in this case because the plain meaning would be inconsistent with the present specification***.

In the present application, the specification discusses one example of a bond pad with an area of about 60 um to 100 um square, although it will be appreciated that bond pads could vary in area, for example depending on the technology node. (See paragraph [0003] of the present application as published U.S. Pub. No. 2005/0127516). Even if Buynoski's metal 1 region was a bond pad according to some interpretation, such an interpretation would be inconsistent with the present specification because the specification discloses a bond pad with a *relatively large area* of about 60um to 100 um square. Again, this 60 um to 100 um square feature is inconsistent with Buynoski's metal 1 interconnect layer, because a square area would significantly "blow-up" the size of an individual cell compared to the use of traditional thin metal 1 interconnect lines. This "blow-up" in area would likely make the cost-point of such an integrated circuit infeasible from a cost-point perspective.

In conclusion, although the pending OA asserts that several features in the prior art are bond pads having individual vias formed thereover, as will be appreciated by a person of ordinary skill in the art and as set forth below, ***these other features are not bond pads having multiple vias thereover.*** Therefore, because this limitation is not established by the prior art of record and because there is no suggestion or motivation to modify the prior art to include this limitation, the applicants request withdrawal of the §103 rejection.

II. REJECTION OF CLAIM 16 UNDER 35 U.S.C. § 103(a)

Claim 16 was rejected under §103(a) as obvious over U.S. Pat. No. 6,545,358 (Jeong) in view of U.S. Pat. No. 6,218,282 (Buynoski) and further in view of U.S. Pat. No. 5,827,782 (Shih). Claim 16 is believed to be patentably distinguishable from the prior art for at least the following reasons.

i. As argued above, the prior art fails to disclose a bond pad having multiple vias formed thereover, as recited in claim 16.

Because this limitation is not established by the prior art of record and because there is no suggestion or motivation to modify the prior art to include this limitation, the applicants request withdrawal of the §103 rejection of claim 16

III. CONCLUSION

For at least the above reasons, independent claims 1 and 16 and all claims depending either directly or indirectly therefrom are believed to be in condition for allowance. Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

In addition, should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 20-0668, TI-36853.

Respectfully submitted,
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Appendix I

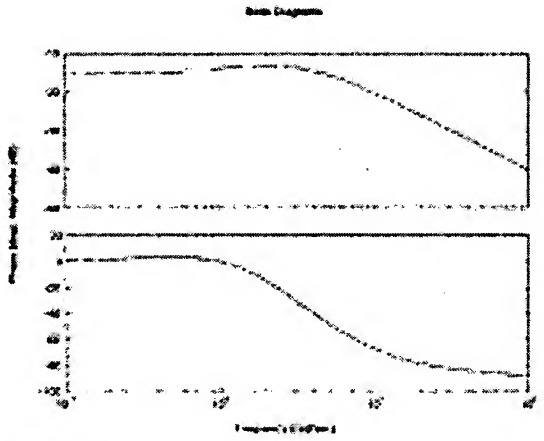
(Dictionary definition of "bond pad" provided by Examiner)

Bode diagram *See* Bode plot.

Bode plot a graphical characterization of the system frequency response: the magnitude of the frequency response $|H(j\omega)|$, $-\infty < \omega < \infty$ in decibels, and the phase angle $\angle H(j\omega)$, $-\infty < \omega < \infty$, are plotted. For example, a system described by the transfer function

$$H(s) = \frac{Y(s)}{F(s)} = \frac{s+1}{(s+2)(s+3)}$$

has the Bode plot shown in the following figure. *See also* frequency response.



Bode plot.

Bode–Fano criteria a set of rules for determining an upper limit on the bandwidth of an arbitrary matching network.

boiler a steam generator that converts the chemical energy stored in the fuel (coal, gas, etc.) to thermal energy by burning. The heat evaporates the feedwater and generates high-pressure steam.

boiling water reactor a nuclear reactor from which heat is transferred in the form of high-pressure steam.

bolted fault a bolted fault is a short circuit fault with no fault resistance. Bolted faults deliver the highest possible fault current for a given location and system configuration, and are used in selecting equipment withstand and interrupting ratings and in the setting of protective relays.

Boltzmann machine in its simplest form, a discrete time Hopfield network that employs stochastic neurons and simulated annealing in its procedure for updating output values. More generally it can have hidden units and be subjected to supervised training so as to learn probabilities of different outputs for each class of inputs.

Boltzmann relation relates the density of particles in one region to that in an adjacent region, with the potential energy between both regions.

bond that which binds two atoms together.

bond pad areas of metallization on the IC die that permit the connection of fine wires or circuit elements to the die.

bonded magnet a type of magnet consisting of powdered permanent magnet material, usually isotropic ceramic ferrite or neodymium-iron-boron, and a polymer binder, typically rubber or epoxy. this magnet material can be molded into complex shapes.

bonding the practice of ensuring a low-resistance path between metallic structures such as water lines, building frames, and cable armor for the purpose of preventing lightning arcs between them.

Boolean an operator or an expression of George Boole's algebra (1847). A Boolean variable or signal can assume only two values: TRUE or FALSE. This concept has been ported in the field of electronic circuits by Claude Shannon (1938). He had the idea to use the Boole's algebra